

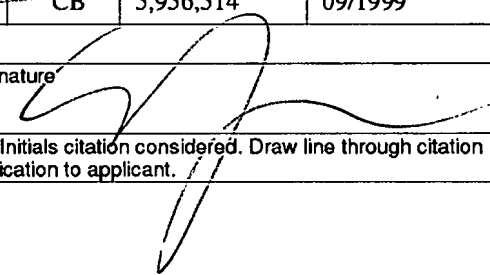
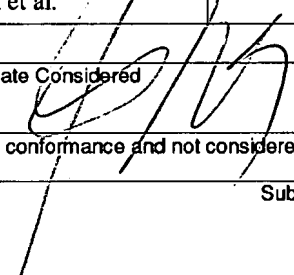
Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-303US1	Application No. 10/069,306
<b>Information Disclosure Statement by Applicant</b> (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant Gilbert Wolrich et al.	
		Filing Date July 3, 2002	Group Art Unit 2183

U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
L	AA	2002/0038403	03/2002	Wolrich et al.			
L	AB	3,577,189	05/1971	Cocke et al.			
L	AC	3,881,173	04/1975	Larsen et al.			
L	AD	4,454,595	06/1984	Cage			
L	AE	4,471,426	09/1984	McDonough			
L	AF	4,477,872	10/1984	Losq et al.			
L	AG	4,569,016	02/1986	Hao et al.			
L	AH	4,742,451	05/1988	Bruckert et al.			
L	AI	4,755,966	07/1988	Lee et al.			
L	AJ	4,808,988	02/1989	Burke et al.			
L	AK	4,816,913	03/1989	Harney et al.			
L	AL	4,847,755	07/1989	Morrison et al.			
L	AM	4,992,934	02/1991	Portanova et al.			
L	AN	5,045,995	09/1991	Levinthal et al.			
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L	AP	5,165,025	11/1992	Lass			
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L	AV	5,394,530	02/1995	Kitta			
L	AW	5,450,603	09/1995	Davies			
L	AX	5,463,746	10/1995	Brodnax et al.			
L	AY	5,509,130	04/1996	Trauben et al.			
L	AZ	5,544,337	08/1996	Beard et al.			
L	BA	5,572,690	11/1996	Molnar et al.			

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h	BC	5,640,538	06/1997	Dyer et al.			
h	BD	5,669,012	09/1997	Shimizu et al.			
h	BE	5,680,564	10/1997	Divivier et al.			
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h	BH	5,748,950	05/1998	White et al.			
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h	BJ	5,812,811	09/1998	Dubey et al.			
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h	BM	5,819,080	10/1998	Dutton et al.			
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h	BX	5,937,177	08/1999	Molnar et al.			
h	BY	5,943,491	08/1999	Sutherland et al.			
h	BZ	5,944,816	08/1999	Dutton et al.			
h	CA	5,946,222	08/1999	Redford			
h	CB	5,956,514	09/1999	Wen et al.			

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2	CD	6,009,505	12/1999	Thayer et al.			
2	CE	6,061,710	05/2000	Eickemeyer et al.			
2	CF	6,139,199	10/2000	Rodriguez			
2	CG	6,141,348	10/2000	Muntz			
2	CH	6,145,123	11/2000	Torrey et al.			
2	CI	6,157,988	12/2000	Dowling			
2	CJ	6,195,739	02/2001	Wright et al.			
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2	CW	6,378,124	04/2002	Bates et al.			
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2	DA	6,408,325	06/2002	Shaylor			
2	DB	6,446,190	09/2002	Barry et al.			
2	DC	6,496,847	12/2002	Bugnion et al.			

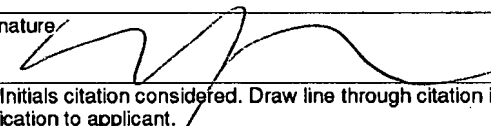
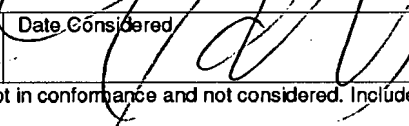
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<i>h</i>	DD	6,523,108	02/2003	James et al.			
<i>h</i>	DE	6,543,049	04/2003	Bates et al.			
<i>h</i>	DF	6,560,629	05/2003	Harris			
<i>h</i>	DG	6,560,671	05/2003	Samra et al.			
<i>h</i>	DH	6,564,316	05/2003	Perets et al.			
<i>h</i>	DI	6,574,702	06/2003	Khanna et al.			
<i>h</i>	DJ	6,697,935	02/2004	Borkenhagen et al.			
<i>h</i>	DK	6,862,676	03/2005	Knapp et al.			
<i>h</i>	DL	6,976,095	12/2005	Wolrich et al.			
<i>h</i>	DM	6,983,350	01/2006	Adiletta et al.			
<i>h</i>	DN	7,020,871	03/2006	Bernstein et al.			


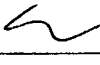

















Foreign Patent Documents or Published Foreign Patent Applications								
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
<i>h</i>	DO	0 130 381	01/1985	Europe				
<i>h</i>	DP	0 463 855	01/1992	Europe				
<i>h</i>	DQ	0 476 628	03/1992	Europe				
<i>h</i>	DR	0 696 772	02/1996	Europe				
<i>h</i>	DS	WO03/019399	03/2003	WIPO				
<i>h</i>	DT	WO03/085517	10/2003	WIPO				

Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Desig. ID	Document
<i>h</i>	DU	"HART, Field Communications Protocol, Application Guide", Hart Communication Foundation, pp. 1-74, (1999).
<i>h</i>	DV	Bowden, Romilly, "What is HART?" Romilly's HART® and Fieldbus Web Site, 3 pages, (1997). <URL: <a href="http://www.romilly.co.uk/whathart.htm">http://www.romilly.co.uk/whathart.htm</a> >
<i>h</i>	DW	Cheng, et al., "The Compiler for Supporting Multithreading in Cyclic Register Windows", IEEE, pp. 57-62, (1996).

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**Other Documents (include Author, Title, Date, and Place of Publication)**

Examiner Initial	Desig. ID	Document
	DX	Hennessy et al., <i>Computer Organization and Design: The Hardware/Software Interface</i> , Morgan Kaufman Publishers, pp. 116-119, 181-182, 225-227, 447-449, 466-470, 476-482, 510-519, 712, (1998).
	DY	Heuring et al., <i>Computer Systems Design and Architecture</i> , Reading, MA, Addison Wesley Longman, Inc., pp. 174-176 and 200, (1997).
	DZ	Heuring et al., <i>Computer Systems Design and Architecture</i> , Reading, MA, Addison Wesley Longman, Inc., pp. 38-40, 143-171, and 285-288, (1997).
	EA	Hidaka, Y., et al., "Multiple Threads in Cyclic Register Windows", <i>Computer Architecture News</i> , ACM, New York, NY, USA, 21(2):131-142, May 1993.
	EB	Hirata, H., et al., "An Elementary Processor Architecture with Simultaneous Instruction Issuing from Multiple Threads", <i>Proc. 19th Annual International Symposium on Computer Architecture, ACM &amp; IEEE-CS</i> , 20(2):136-145, May 1992.
	EC	Intel, "IA-64 Application Developer's Architecture Guide," Rev.1.0, pp. 2-2, 2-3, 3-1, 7-165, C-4, and C-23, May 1999.
	ED	Jung, G., et al., "Flexible Register Window Structure for Multi-Tasking", <i>Proc. 24th Annual Hawaii International Conference on System Sciences</i> , vol. 1, pp. 110-116, (1991).
	EE	Koch, G., et al., "Breakpoints and Breakpoint Detection in Source Level Emulation", <i>Proc. 19th International Symposium on System Synthesis (ISSS '96)</i> , IEEE, pp. 26-31 (1996).
	EF	Moors, et al., "Cascading Content-Addressable Memories", <i>IEEE Micro</i> , 12(3):56-66 (1992).
	EG	Okamoto, K., et al., "Multithread Execution Mechanisms on RICA-1 for Massively Parallel Computation", <i>IEEE - Proc. Of PACT '96</i> , pp. 116-121 (1996).
	EH	Patterson, et al., <i>Computer Architecture A Quantitative Approach</i> , 2nd Ed., Morgan Kaufmann Publishers, Inc., pp. 447-449, (1996).
	EI	Paver, et al., "Register Locking in an Asynchronous Microprocessor", <i>IEEE</i> , pp. 351-355, (1992).
	EJ	Philips ED - Philips Components: "8051 Based 8 Bit Microcontrollers, Data Handbook Integrated Circuits, Book IC20", 8051 Based 8 Bit Microcontrollers, Eindhoven, Philips, NL, pp. 5-19 (1991).
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	EL	Quammen, D., et al., "Flexible Register Management for Sequential Programs", <i>IEEE Proc. of the Annual International Symposium on Computer Architecture</i> , Toronto, May 27-30, 1991, vol. SYMP. 18, pp. 320-329.
	EM	Ramsey, N., "Correctness of Trap-Based Breakpoint Implementations", <i>Proc. of the 21st ACM Symposium on the Principles of Programming Languages</i> , pp. 15-24 (1994).
	EN	Steven, G.B., et al., "ALU design and processor branch architecture", <i>Microprocessing and Microprogramming</i> , 36(5):259-278, October 1993.
	EO	Young, H.C., "Code Scheduling Methods for Some Architectural Features in Pipe", <i>Microprocessing and Microprogramming</i> , Elsevier Science Publishers, Amsterdam, NL, 22(1):39-63, January 1988.
	EP	Young, H.C., "On Instruction and Data Prefetch Mechanisms", <i>International Symposium on VLSI Technology, Systems and Applications, Proc. of Technical Papers</i> , pp. 239-246, (1995).

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